ABSTRACT OF THE DISCLOSURE

There is provided a logic verification system having improved development time and design quality, in which all pins of an FPGA module are wired in direct between the FPGA module and a bridge circuit used in the verification processes of a logic simulator accelerator and a logic emulator, a cutting end of the verification object logic is assigned to an external interface connector of the FPGA module when the logic simulation is accelerated, and the correspondence between each pin of external interface connector of the FPGA module and logic signal is performed on the logic simulator on the general purpose processor.